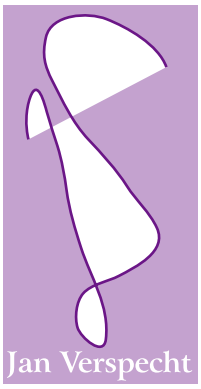

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Load-pull measurement of transistor negative input impedance

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Load-pull measurement of transistor negative input impedance

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***Abstract* — This paper presents a measurement-based way of forecasting some transistor's nonlinear effects. For some particular output impedances of the passive load-pull setup, a strange behavior of the Pout/Pin slopes can be obtained. Thanks to the LSNA, the non linear input impedance can be measured, it is useful to explain this phenomenon. The time domain slopes of a GaN HEMT up to 3.5 W/mm are proposed at these particular loci.**

***Index Terms* — active circuits, input impedance, LSNA, nonlinearities, power measurement.**

I. Introduction

RF designers need to design their circuits with a guaranteed stability. Even if load-pull measurements are well suited to know the best load impedance [1] [2], the real operation load impedances can widely change. Thus the knowledge of the transistor behavior versus load impedance is required, especially for stability and reliability purposes [3] [4] [5].
This paper will present the measured effect of some particular load impedances on a GaN HEMT, resulting in a strong feed-back at the input side. In-depth investigations and comparisons will be proposed, in order to point out the phenomenon.

II. Description of the Observed Phenomenon

The setup used for these measurements was described in [6]. It is based on the LSNA and passive tuners, with a nice feature: the incident and reflected wave measurements are taken very close to the device, before the tuners and with neglectable losses. As a consequence, the LSNA calibration does not depend on the tuner settings.
The DUT is a GaN HEMT grown on SiC substrate and processed by Thales-Tiger (France); size: 2x100 µm (grid length: 0.25 µm, pitch: 35 µm); bias (without RF) Vgs=-4V, Vds=20V, Id=65mA. The frequency is 4 GHz CW, four harmonic frequencies are taken into account for the time domain measurements. Three measurement points will be considered:

- The Fig. 1 shows a sweep of input power for a given load impedance : Z_{load_1}=(214.2+j21.2)Ω. The maximum output power is 0.684W (power density 3.42W/mm).
- The Fig. 2 gives the results obtained for an other load impedance Z_{load_2}=(123.9+j92.4)Ω. The same maximum output power of 0.694W is reached. But this slope shows that for a given input power, a strange behavior appears and the power gain strongly increases.
- The Fig. 3 proposes the same measurement for the load impedance Z_{load_3}=(164.9+j124.9)Ω. The maximum output power is now 0.692W. But the slope is now hectic, with several strange points.

The Figs 1, 2, 3 propose the Pout/Pin ratio at the fundamental frequency. Note that the power measurements at both ports are performed with the LSNA, the source impedance is 50 Ohms. A close look to a1 and b1 (the incident and reflected waves at port 1 at f0) shows some areas where b1(dBm)>a1(dBm) (because of LSNA computation, Pin is a combination of two slopes : dBm(Pin) for positive Pin and dBm(-Pin) for negative Pin). The LSNA provides separately the incident and reflected components at both ports. Thus, the DUT input power is precisely known. Besides, Fig. 4, 5 give corresponding time domain slopes for case 2, 3 respectively. They show that the observed phenomenon is difficult to detect without complete computation of incident and reflected power levels at the fundamental frequency.

III. Determination of the Cause and Influence of Load Impedance

Different causes can explain a strange Pout/Pin slope: a real device instability, or an error of the measurement setup.
In order to reach a maximal confidence on the measured data, several verifications have been performed with the measurement setup :

- Calibration drift issue: The LRRM absolute calibration [7] has been checked-up, it has been verified that it is sufficiently stable for a week ;
- Calibration algorithm issue: we have verified the power levels provided by the LSNA with a power meter, a good agreement has always been obtained ;
- Oscillation at any other frequency, not seen by the LSNA: the load is replaced by an attenuator and an analog spectrum analyzer, no unattended spectrum line has been seen in IF and RF band, even in the worst case of strange measurement.

As a consequence, this strange Pout/Pin slope does not correspond to a problem of the setup, and no more to an oscillation.

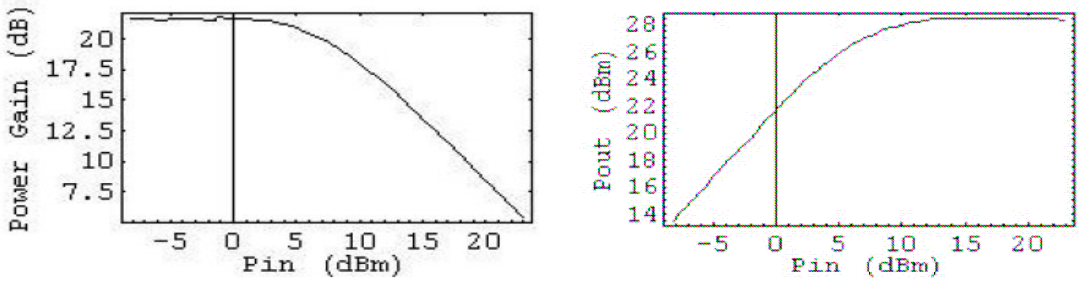

Fig. 1 : Power gain (left) and output power (right) versus input power for case 1, Z_{load_1}=(214.2+j21.2)Ω

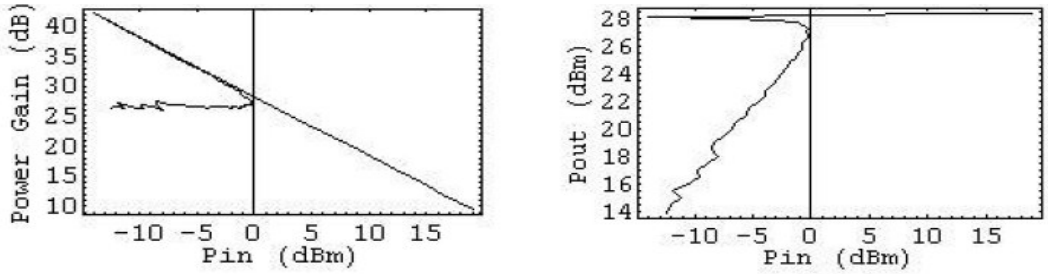

Fig. 2 : Power gain (left) and output power (right) versus input power for case 2, Z_{load_2}=(123.9+j92.4)Ω

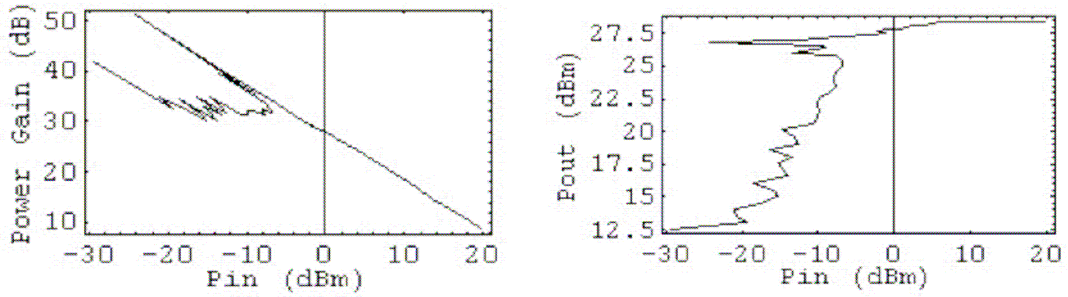

Fig. 3 : Power gain (left) and output power (right) versus input power for case 3, Z_{load_3}=(164.9+j124.9)Ω

Now, thanks to the vector measurements at both device sides, we can look at the variation of the input impedance for a given output impedance. The Fig. 6, 7, 8 show the input impedance of the case of Figs. 1, 2, 3 respectively. These input impedances are measured at the fundamental frequency, and given at the same input powers than Figs. 1, 2, 3. We can see that:

- On Fig. 6, every point gives an input impedance which has a positive real part, it means the locus is always in the Smith chart.
- The Fig. 7 shows that the input impedance has a negative real part for small signals, and it becomes equal to zero for a higher input power. So the input power decreases hardly because the transistor input reflects nearly all the energy. Thus the Pout/Pin ratio suddenly becomes very large.
- The Fig. 8 behaves like Fig. 7, but the device input impedance has a real part close to zero for many working points.

These cases show that several values of the load impedance induce this phenomenon. The Fig. 9 shows the relevant areas.

It is visible that a small variation of the output tuner in phase and/or in amplitude can totally change the nonlinear behavior of the transistor. One must note that the RF source impedance was always 50 Ohms, so the particular working points shown in this paper do not have destroyed the DUT. If one tries to tune in such configurations the source impedance for optimal input power, then the DUT will certainly oscillate and be damaged.

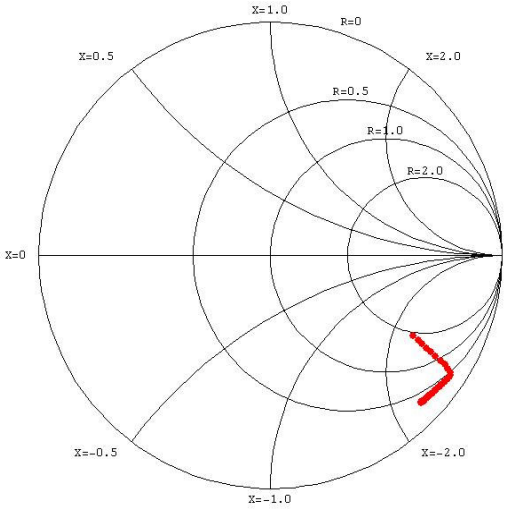

Fig. 6 : input impedance for different input powers for case 1: every point in the Smith chart

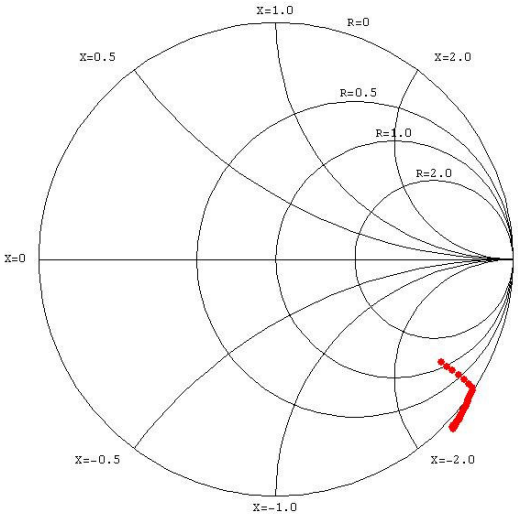

Fig. 7 : input impedance for different input powers for case 2: first points not in the Smith chart

This measurement result looks strange, it can be explained by taken into account the nonlinear behavior of transistors. This phenomenon can be observed within a nonlinear circuit simulator, and with many FET devices.

V. CONCLUSION

We have obtained some negative Pout/Pin slopes, it is shown that these measurement results make sense due to the nonlinear nature of transistors. For some particular load impedances, the DUT exhibits a small or negative real part of input impedance. A 50 Ohms source impedance allows to characterize these areas with a reasonable safety in a load-pull environment.

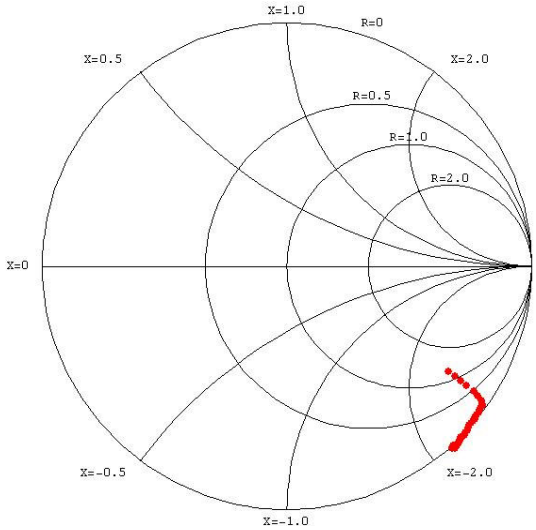

Fig. 8 : input impedance for different input powers for case 3: first points very close to the limit of the Smith chart

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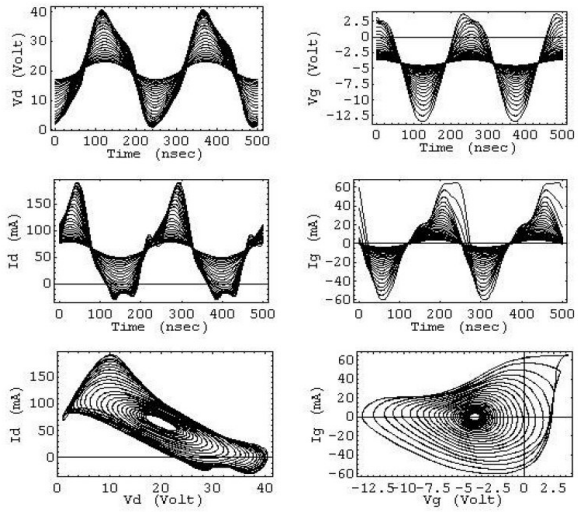

Fig. 4 : Time domain slopes for case 2, $Z_{load\_2}=(123.9+j92.4)\Omega$

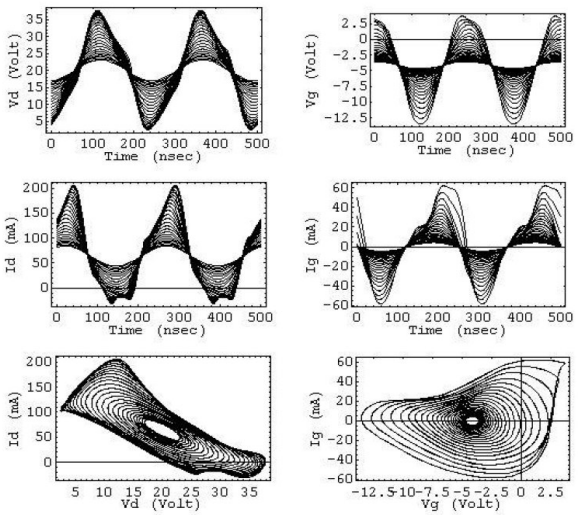

Fig. 5 : Time domain slopes for case 3, $Z_{load\_3}=(164.9+j124.9)\Omega$

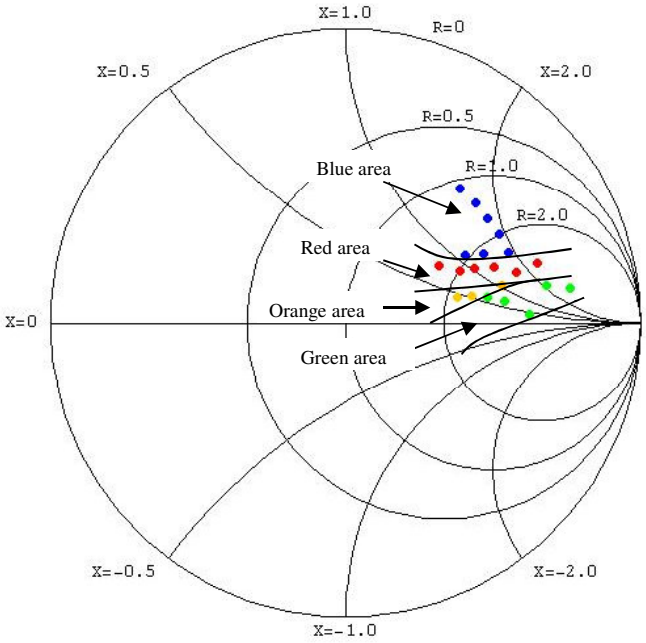

Fig. 9 : different load impedances for an input power sweep :

- green : no strange power gain (case 1)
- blue : presence of a strange power gain for a input power (case 2)
- red : presence of strange power gain for a lot of input powers (case 3)
- orange : between case 2 and case 3